Partial English Translation of

LAID OPEN unexamined

JAPANESE PATENT APPLICATION

Publication No. 10-12568

[0032] to [0039]

[0032]

[Embodiment]

<First Embodiment> An embodiment of the present invention will be explained with reference to Figures 6 to 15.

[0033] Firstly, the configuration and the structure of the memory cell array part of a DRAM device will be explained with reference to Figure 6 and Figure 7. A region where the source, the drain and the channel of the MOSFET are formed is indicated by a region encircled by a line 20. The gate electrode of the MOSFET, which serves as the word line of the memory cell array, is indicated by a region encircled by a line 21, and a region to serve as the bit line of the memory cell array is indicated by a region encircled by a line 22. Figure 7(a), Figure 7(b) and Figure 7(c) show respective cross-sectional views of Figure 6 along a line a-a, a line b-b and a line c-c. The MOSFET is formed in a region of a p-type silicon substrate 23, which is surrounded by an insulating film 24, and includes a diffusion layer 25 as the source and the drain, a gate insulting film 26 and a gate electrode 27 covered with an insulating film 28. A metal silicide layer 29 is formed in an exposed surface of the diffusion layer 25 and a conductive film 30 is formed on the silicide layer 29. The conductive film 30 is surrounded by an insulating film 31.

[0034] Further, a metal silicide layer 32 is formed on the surface of the conductive film 30, and a wiring 33 to serve as the bit line is formed on the respective surfaces of the silicide layer 32 and the insulating film 28.

The peripheral region of the bit line wiring 33 is covered with an insulating film 34.

[0035] A conductive film 35 is formed on the silicide layer 30, the insulating film 31 and the insulating film 34, and is surrounded by an insulating film 36. An electric charge storage electrode 37 is connected to a conductor 35, and a capacitor insulating film 38 and a plate electrode 39 are formed on or over the respective surfaces of an electric charge storage electrode 37 and an insulator 36 so that a capacitor is formed.

[0036] The memory cell shown in Figure 7 is formed in the following procedures. Firstly, as shown in Figure 8, an element isolation region is formed in a manner that the insulating film 24 is filled in a trench having a depth of 0.25 μm and formed in the p-type silicon (Si) substrate 23 of which acceptor has a concentration of $3 \times 10^{16}/cm^3$. This trench is formed by the well known dry etching. After a thermal oxide film is formed to 10 nm on the side faces and the bottom face of the trench, a Si oxide film is deposited to 30 nm by a generally-performed CVD method to planarize the surface thereof.

[0037] A p-type buried conductive layer is formed in the Si substrate 23 so that a depth thereof is 0.4 μm, the maximum concentration of the acceptor is $3 \times 10^{17}/cm^3$ and the standard deviation of distribution is 0.08 μm. Thereafter, as shown in Figure 9, the gate oxide film 26 made of a Si oxide film and having a thickness of 10 nm and a gate electrode 27 made of a n-type polycrystal Si film and having a thickness of 150 nm are formed.

[0038] Next, after the diffusion layer 25, of which surface has a concentration of $1 \times 10^{19}/cm^3$ and which has a depth of 100 nm, is formed as the source/drain, a sidewall 28 made of a Si oxide film and having a thickness of 100 nm is formed.

[0039] Further, after a cobalt film having a thickness of 10 nm is formed and a silicide layer is formed on the exposed surface of the diffusion layer

25 by a thermal treatment at a temperature of 600 ℃ for 60 seconds, non-reacting cobalt films on the Si oxide films 28 and 24 are removed. Subsequently, the resistance of the cobalt silicide layer is made low by a thermal treatment at a temperature of 700 ℃ for 30 seconds, and a cobalt silicide layer 29 having a thickness of 25 nm is formed on the exposed surface of the diffusion layer 25.